USE OF PSEUDO EXHAUSTIVE TEST PATTERN GENERATOR ON THE BASIS OF SHIFT REGISTERS WITH NONLINEAR FEEDBACK

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In recent years considerable attention has been given to pseudoexhaustive testing of a combination circuit. This approach involves applying all possible input patterns to all individual output cones. An output cone consists of all gates that feed the output. Pseudoexhaustive testing allows to reduce test time, to implement self-test architecture using signature or syndrome compression and ensures detection of all detectable combinational faults in the circuit. This approach does not require test generation based on programmed techniques and test evaluation associated with the use of fault simulator to assess fault cover.

Several approaches to the pseudoexhaustive testing have been proposed. Pseudoexhaustive test pattern generators (TPG) are usually based on maximal length LFSR. An n-stage maximal length LFSR has a period of 2n-l states and utilizes a primitive polynomial for its feedback connections. Universal pseudoexhaustive TPG generates test containing n- tuples that cover any "k" columns of the exhaustive test sets of all 2k possible patterns. This test sets can be generated by LFSR based on linear codes or constant weight codes. Specific TPGs such as LFSR/SRs and LFSR/XORs can be designed for (n, m, k) circuit by using the knowledge of the circuit output cones. An LFSR/SR consists of an LFSR and a shift register (SR) and can be realized with low hardware overhead. The pseudoexhaustive test set generated by LFSR/SR is often significantly greater than the bound (2k). An LFSR/XOR is composed of an LFSR and an XOR gates and requires high hardware overhead. The TPG design procedures based on convolved LFSR/SR are presented in. We present our TPG designs that generate pseudoexhaustive test by utilizing nonlinear feedback shift register (NLFSR) for the generation of full-length shift-register cycles, also referred to as de Bruijn sequences. We propose algorithmic method of constructing full-cycles by using fan out free cascade arrays as the nonlinear feedback of the shift register. We have designed various pseudoexhaustive TPGs for examples of the combinational circuits from papers. For these circuits TPGs utilizing NLFSR require less test size and hardware overhead.

We have presented new hardware efficient TPG design to generate minimal pseudoexhaustive test sets for combinational circuit. These TPGs utilize the information about output cone dependences and generate pseudoexhaustive test sequences using non-linear feedback shift registers. This technique has great potential to generate minimum test sets as demonstrated by the examples of (n,m,k) circuits and to design of the TPGs with self-checking properties.