

HARDWARE COMPUTATIONAL INFRASTRUCTURE FOR BOOLEAN NETWORK ATTRACTORS SEARCH

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One of the approaches in the search for treatment of complex diseases, such as T-cell leukemia of large granular lymphocytes, various cancers and autoimmune diseases, is the analysis of gene expression sequences – gene regulatory networks (GRN). The main method used, which has proved its effectiveness in applied research, is Boolean Networks model construction [1]. It is based on the ambivalent behavior of a gene: a gene can be activated (equivalent to a boolean state of "True" or 1) or remain inactive (equivalent to a boolean state of "False" or 0). When activated, a gene triggers chemical processes that, in turn, can trigger the expression or suppress the expression of other genes in a temporal sequence. Such behavior can be described by the corresponding boolean expressions, and the whole process in time is described by a deterministic or probabilistic finite state machine (FSM) model with a synchronous or asynchronous mode of operation, depending on the required accuracy of correspondence to real biological processes.

The main task in the study of gene co-expression networks is the search for attractors – closed cycles, to which sequences of processes occurring inside cells converge [2]. The computational task of finding all attractors in networks that include dozens of genes is extremely hard. It belongs to the class of NP-hard problems. This means that there is no efficient way to find all attractors in polynomial time.

At the moment, a large number of software tools have been developed [3], which allow you to define and simulate Boolean Networks: to study their static and dynamic properties, to search for stable states and attractors, to study the influence of disturbing factors (interventions) on the network operation. Despite the possibility of studying Boolean Networks of a sufficiently large size (they can include dozens of genes), all software tools have a significant drawback: for an exhaustive study of a large Boolean network model, it is necessary to spend considerable time, in view of the sequential nature of calculations on general-purpose computers.

Since Boolean network models can be described as finite state machine model, hardware accelerators implemented using FPGA can be used to study them in order to find attractors [4, 5]. The use of FPGA allows not only to create a specialized computing hardware that will effectively analyze the Boolean network model in order to search for attractors, but also allows you to create an array of

such computing elements in order to significantly speed up the analysis process due to their simultaneous operation.

In this paper, we propose a model of an efficient reconfigurable hardware accelerator for implementation on an FPGA, with which you can significantly speed up finding the set of attractors of an arbitrarily given Boolean network. The structure of the proposed accelerator is shown in the figure:

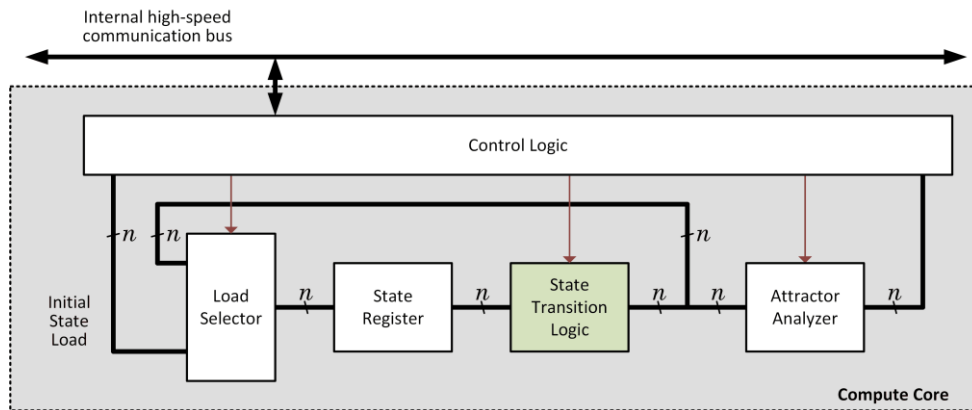


Figure 1

It includes the Control Logic block and the Datapath. The Datapath is an implementation of the synchronous state propagation model in a Boolean network in the form of a Moore state machine. The main elements of the model are a reconfigurable State Transition Logic module and an Attractor Analyzer. The main feature of the accelerator is the ability of the transition logic between states to be reconfigured by demand, which eliminates the need to perform complex and very time-consuming processes of technological project preparation to change the implemented Boolean network model.

References:

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